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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/512,017	04/29/2005	Thomas Benetik	10808/169	8467

48581 7590 10/15/2009

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EXAMINER	
CHIU, TSZ K	

ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
10/15/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/512,017	BENETIK ET AL.	
	Examiner	Art Unit	
	Tsz K. Chiu	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *49* is/are allowed.

6)☒ Claim(s) *21-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

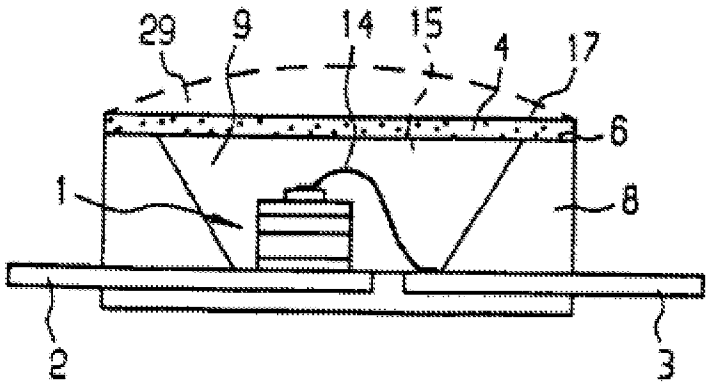
Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 21-48 have been considered but are moot in view of the new ground(s) of rejection. Applicant argues that Vathulya fails to disclose the top wall side walls are directly covered by the insulating layer, however Vathulya shows in figures 3 and 4 that elevation portion 32 is surrounded on the left and right side by the insulating layer (27-30) and the top most elevation is directly covered by layer 30. Therefore, the rejection is proper. (top wall are directly covered by the insulating layer can also interpret as see drawing below, the layer 6 is directly covered the LED device 1).



Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 21, 23-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Vathulya et al. (6297524).

In re claims 21,38 and 48, Vathulya discloses a capacitor (Figs. 3 and 4) that contain an insulating layer (27-30) disposed on a semiconductor substrate (21) and a capacitance structure formed in the insulating layer, the structure having two capacitance surface parts, the first capacitance surface part having at least a first metallization plane (22) and a second metallization plane (23) extending approximately parallel to the substrate surface and are each operatively connected to one of two electrodes (A/B) and the second capacitance surface part having at least one electrically conductive region (32) between the first metallization plane and the second metallization plane in the insulating layer and is operatively connected to one of the first metallization plane and the second metallization plane where the second capacitance part is in the form of a homogenous cohesive elevation and where the elevation comprises a top wall and side walls, wherein the top wall is oriented perpendicular to the side walls and wherein the side walls and the top wall are directly covered by the insulating layer. (As seen the elevation portion 32 is surrounded on the left and right side by the insulating layer (27- 30) and the top most elevation is covered by layer 30)

In re claim 23, the electrically conductive region of the second capacitance part is arranged at about a right angle to the first metallization plane and the second metallization plane. (Fig. 4)

In re claim 24, the electrically conductive regions is divided into at least two parts, a first conductive region (#32, vias 1,3,5,7,9) and the second conductive region (#32, vias 2,4,6,8) and

the first conductive region is operatively connected to the first metallization plane and the second conductive region is operatively connected to the second metallization plane. (Fig. 3)

In re claim 25, the metallization planes are in the form of cohesive plate. (Fig. 4)

In re claim 26, the first conductive region further comprises a first plurality of conductive bars forms (32) and the second conductive regions comprise a second plurality of conductive bar forms (32).

In re claim 27, the first plurality of bar forms are arranged at a fixed distance from one another on the first metallization plane and extends in the direction of the second metallization plane and the second plurality of bar forms are arranged at a fixed distance from one another on the second metallization plane and extends in the direction of the first metallization plane. (Fig. 3-4)

In re claim 28, the first plurality of bar forms has a first length and the second plurality of bar forms has a second length and the first length is greater than, less than or the same length as the second length and the sum of the first length and the second length is greater than a distance between the first metallization plane and second metallization plane. (Fig. 3)

In re claim 29, the at least one of the first metallization plane and the second metallization is comprised of at least two electrical lines (32) in parallel to one another and the electrical lines of the first metallization plane are arranged congruently with respect to the electrical lines of the second metallization plane.

In re claim 30, the electrically conductive region is divided into at least two parts, a first conductive region (32, vias 1,3, 5, 7, 9) and a second conductive region (32, vias 2, 4, 6, 8) and the first conductive region is operatively arranged on the electrical lines of the first metallization

plane and the second conductive region is operatively arranged on the electrical lines of the second metallization plane.

In re claim 31, the first conductive region further comprises a first plurality of conductive bar forms (32) and the second conductive region further comprises a second plurality of conductive bar forms (32).

In re claim 32, the first plurality of bar forms are arranged at a fixed distance from one another on the first metallization plane and extends in the direction of the second metallization plane and the second plurality of bar forms are arranged at a fixed distance from one another on the second metallization plane and extends in the direction of the first metallization plane. (Fig. 3-4)

In re claim 33, the first plurality of bar forms has a first length and the second plurality of bar forms has a second length and the first length is greater than, less than or the same length as the second length and the sum of the first length and the second length is greater than a distance between the first metallization plane and second metallization plane. (Fig. 3)

In re claim 34, the first metallization plane is in the form of a cohesive plate and the second metallization plane is a lattice. (Fig 4)

In re claim 35, the electrically conductive region is operatively attached to the first metallization plane and further comprises a plurality of bar forms (32) extending in the direction of the second metallization plane and at least on e bar of the plurality of bars projects at least partially into a cutout in the lattice. (Fig. 4)

In re claim 36, a third metallization plane (L3) in a form of a lattice and arranged in parallel to and at a distance from the second metallization plane and the second and third metallization planes are electrically connected to one another. (Fig. 3)

In re claim 37, at least one of a plurality of bar forms project through the cut-out in the metallization plane and extend at least partially into a cut-out in the third metallization plate. (Fig. 3)

In re claim 39, the electrically conductive region is formed in a homogenous cohesive elevation, the region being formed between at least two metallization planes (22, 23), which are formed by patterning the metallization plane.

In re claim 40, forming electrically conductive region in the insulating material (27) as a via structure (32).

In re claim 41, the via structure arranges the electrically conductive region at essentially a right angle to the metallization planes. (Fig. 3)

In re claim 42, the via structures form bars (32) that are operatively connected to the first metallization plane extending towards the second metallization plane.

In re claim 43, forming the first metallization plane and the second metallization plane as cohesive plates. (Fig. 4)

In re claim 44, forming the first metallization plane as at least two electrical lines (32, vias 1,3, 5, 7, 9) arranged in parallel to one another and the second metallization plane as at least two electrical lines (32, vias 2, 4, 6, 8) parallel to one another and the electrical lines of the first metallization are congruently arranged with respect to the electrical lines of the second metallization plane.

In re claim 45, forming the first metallization plane as a cohesive plate and the second metallization plane as a lattice. (Fig. 3, 4)

In re claim 46, forming a third metallization plane (L3) as a lattice. (Fig. 3)

In re claim 47, forming a via (32) arrangement that forms a bar (32) extending from the first metallization plane through a cutout of the second metallization plane and extending into a cutout in the third metallization plane. (Fig. 3)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Vathulya.

In re claim 22, Vathulya discloses all the limitations except for the electrically conductive regions of the second capacitance part formed by a damascene process. This limitation is a product by process limitation. A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao and Sato et al., 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also In re Brown and Saffer, 173 USPQ 685 (CCPA 1972): In re Luck and Gainer, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and In re Marosi et al., 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear. Even though product -by [-]

process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted)."

Allowable Subject Matter

Claim 49 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: Claim 49 is allowable over the reference of record because none of these references discloses or can be combined to yield the claimed invention of a capacitance structure wherein the insulating layer is in between the top wall and the one of the first metallization plane and the second metallization plane that is not connected to the electrically conductive region of the second capacitance part.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsz K. Chiu whose telephone number is 571-272-8656. The examiner can normally be reached on 0800 to 1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/
Supervisory Patent Examiner, Art Unit 2822

/Tsz K Chiu/

Examiner, Art Unit 2822

October 12, 2009